ABSTRACT

A path delay measuring circuitry includes a pattern creating circuit 105 for creating a test pattern to be supplied to a combination circuit 101, a comparison/decision circuit 106 for comparing an output from the combination circuit and an expected value, a clock creating circuit 301 for creating a clock with a variable clock interval while a capturing operation is carried out according to a clock mode value, and a timing signal creating circuit 107 for supplying an operation timing signal to each of the respective circuits. The clock generating circuit 301 includes a clock mode counter for producing a clock mode value which is updated whenever a decision for signal transition time is made.

[Selected Drawing] Fig. 3